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APPLICATION FOR LETTERS PATENT

FOR

LDMOS TRANSISTOR

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LDMOS TRANSISTOR

FIELD OF THE INVENTION

The present application relates to an LDMOS transistor structure.

BACKGROUND OF THE INVENTION

LDMOS transistor structures are widely used in semiconductor devices for many types of transistor applications such as high voltage MOS field effect transistors. An LDMOS transistor comprises a lightly doped drain region to enhance the breakdown voltage. Fig. 1 shows a top view of a combined transistor structure including two MOSFET transistors. Both transistors are arranged within an active, for example, p doped area 1 that is isolated from the surroundings, by a so-called field region 11. The transistors share a common drain region consisting of a n+ doped region 9 surrounded by a n^- doped region 8. Two source regions 6, 7 are arranged on the left and the right side of this drain region 8, 9. Thus, two channels are defined by the drain region 8, 9 and the two source regions 6 and 7, respectively. The broken lines indicate the gates 4 and 5 which are arranged above these channels. To the left and the right of the source regions 6 and 7, there are arranged p^+ sinker structures 2 and 3 which extend from the surface of epitaxial layer to the bottom of the substrate to provide for a source connection on the backside of the substrate.

The active region 1 can be enclosed by a single step, the LOCal Oxidation of Silicon (LOCOS) as known in the art. This process creates a so called high stress field oxide bird's beak region which in combination with the p^+ sinker structure implants 2 and 3 can result in a leakage path between the n^+ drain and the p^+ sinker structure along the interface stress and implant damage induced defect centers as indicated by arrows 10.

The conventional solution to prevent such a leakage is to increase the spacing between p^+ and n^+ implants to the bird's beak to suppress the leakage current.

The disadvantages of such a measurement is, however, the increase of the non- functional part of the transistor fingers and the reduction of the isolation region.

SUMMARY OF THE INVENTION

According to the present application, a new transistor structure is introduced which avoids such a leakage.

A semiconductor device comprises an active region of a first conducting type including a transistor structure, and a ring shaped region of the first conducting type extending from a surface of the active region into the active region and substantially surrounding the transistor structure.

The transistor structure may comprise, a drain region, a source region, wherein the drain and the source define a channel, a gate being arranged above said channel, and a sinker structure of said first conducting type arranged substantially along said source region reaching from the surface of the active area next to the source region to the bottom of the active area. The p ring can be less doped than the sinker structure. The device may further comprise a metal layer on the backside of the semiconductor device. The transistor structure can be a two transistor structure comprising, a common drain region, a first source region arranged on one side of the common drain region, a second source region arranged on the respective opposite side of the drain region, wherein the drain region and the source regions each define a channel, a first and second gate being arranged above said channels, and a first and second sinker structure of said first conducting type arranged substantially along said source regions reaching from the surface of the active area next to the respective source regions to the bottom of the active area. The drain region may comprise a lightly doped drain region. The ring can be doped in the range of 10^{14}-10^{15}/cm^2. The active area can be created and enclosed by a LOCOS process. The active area may comprise a substrate and an epitaxial layer on top of said substrate. The first conducting type can be the p type or n type. The ring can be created by masked ion implant. Boron can be used as a dopant. The

ring may have a rectangular, circular, oval, or polygon shape. The ring may comprise at least one gap that does not substantially influence an insulating function of the ring.

According to another embodiment, a semiconductor device comprises an active region of a first conducting type including a transistor structure, wherein the transistor structure comprises, a drain region of a second type, a channel, and a gate being arranged above said channel, and a ring shaped region of the first conducting type extending from a surface of the active region into the active region and surrounding the transistor structure.

The device may further comprise a source region of the second type arranged along one side of the drain region, and a sinker structure of said first conducting type arranged substantially along said source region reaching from the surface of the active area next to the source region to the bottom of the active area. The device can also further comprise a second source region arranged on the respective opposite side of the drain region, wherein the drain region and the source regions each define a channel, a first and second gate being arranged above said channels, and a first and second sinker structure of said first conducting type arranged substantially along said source regions reaching from the surface of the active area next to the respective source regions to the bottom of the active area. Again, the drain region may comprise a lightly doped drain region and the device may further comprise a metal layer on the backside of the semiconductor device. The ring may be less doped than the sinker structure and can be doped in the range of 10^{14}-10^{15}/cm^2. The active area can be created and enclosed by a LOCOS process. The active area may comprise a substrate and an epitaxial layer on top of said substrate. The first conducting type can be the p type or n-type. The ring can be created by masked ion implant. Boron can be used as a dopant. The ring may have a rectangular, circular, oval, polygon, or partially open shape. The ring may further comprise at least one gap that does not substantially influence an insulating function of the ring.

A method of manufacturing a semiconductor device comprises the steps of:

- forming an active region of a first conducting type within a semiconductor material;

- forming a transistor structure, and

- forming a ring shaped region of the first conducting type extending from a surface of the active region into the active region and surrounding the transistor structure.

The step of forming a transistor structure may comprise the steps of forming a drain region of a second type, a source region of the second type arranged along one side of the drain region, and a sinker structure of said first conducting type arranged substantially along said source region reaching from the surface of the active area next to the source region to the bottom of the active area. The method may further comprise the step of forming a second source region arranged on the respective opposite side of the drain region, and a first and second sinker structure of said first conducting type arranged substantially along said source regions reaching from the surface of the active area next to the respective source regions to the bottom of the active area. The drain region can be formed in such a way that it comprises a lightly doped drain region. The method may further comprise the step of arranging a metal layer on the backside of the semiconductor device. The step of forming the ring may include the step of doping the ring less than the sinker structure. The ring can be doped in the range of 10^{14}-10^{15}/cm^2. The active area can be created and enclosed by a LOCOS process. The ring can be created by masked ion implant. Boron may be used as a dopant. The ring can have a rectangular, circular, oval, polygon, or partially open shape.

Other technical advantages of the present disclosure will be readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present disclosure and advantages thereof may be acquired by referring to the following description taken in conjunction

with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

Figure 1 is a top view of a combined transistor structure enclosed by a LOCOS area according to the prior art;

Figure 2 is a top view of a combined transistor structure enclosed by a LOCOS area according to an embodiment of the present invention;

Figure 3 is a sectional view along the line 3-3 in figure 2.; and

Figure 4 shows different possible shapes of the inter unit cell ring.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning to the drawings, an exemplary embodiment of the present application will now be described. Figure 2 depicts a similar transistor structure as shown in figure 1. This figure only shows the drain region and indicates the, sinker, the source region, and the gates by broken lines. Similar structures and elements carry similar numerals. Within the active area 1, an additional p doped ring structure 20 is implanted that extends from the surface of the active area 1 into the epitaxial layer to additionally isolate transistor structures as will be shown in more detail in Fig. 3. Figure 2 shows the p doped ring as rectangular ring structure with two parallel "vertical" areas 22 and two parallel "horizontal" areas 21. However, other forms, such as a circle, oval, hexagonal, or any other polygon shape can be used. The such formed inter-unit cell p ring 20 completely surrounds both transistors. The p ring profile can be generated by masked ion implant, for example, with a boron dose in the range of 10^{14}-10^{15}/cm^2. The inter-unit cells p ring, thus, is created with a lower dose than the p^+ sinker and is used to terminate the electrical field (depletion region) at the end of the unit cells to prevent the electrical field to come in contact with the defect centers, thus limiting the leakage current and providing the leakage current insulating function. The lower dose p ring design reduces the implant damage, improves the source resistance, and suppresses the snapback behavior

For a conventional device, the depletion edge extends along the end of the drain fingers 8, 9 with increasing drain bias. A drain to source leakage path can be formed when the depletion region, in case of an electrical field>0, starts covering the stress and implant damage induced defect centers. As stated above, the inter-unit cells p ring terminates the electrical field (depletion region) at the end of unit cells and effectively prevents the electrical field to come in contact with the defect centers and, thus, suppress the leakage current.

Figure 3 shows the P ring profile within the transistor structure in a sectional view along the line 3-3 of figure 2. However, only a partial view is presented and, thus, only the left transistor is shown in this figure. A wafer comprises for example an active p-area created by the LOCOS process which includes n-type areas 8, 9 and 34 implanted on the surface to provide a drain and source region, respectively. The backside of the substrate comprises a wafer backside metal layer 30 which can be made of gold or aluminum and is used for contact purposes. The area 1 is usually covered with an insulator layer 31 such as silicon oxide in which a polysilicium gate 4 is arranged to cover the channel between the drain region 8 and source region 34. On top of this layer is usually a passivation layer (not indicated in Fig. 3). The source 34 in this exemplary LDMOS transistor can be additionally surrounded by a p doped well 35 depending on what type of technology is used. Electrodes 33 and 32 made of gold or aluminum or any other suitable metal reach through the insulating layer 31 to provide respective couplings between runners for the drain and the source regions, respectively. Runners can also be contacted with the respective drain, source and gate regions by other suitable means, such as, vias or similar coupling structures. To generally reduce a feedback capacitance, the source runner 33 is here extended to cover the gate 4 as shown in Fig. 3. Such a so called field plate over the gate 4 effectively decouples the gate drain capacitance C_{gd} between the gate and the drain. However, other embodiments for the runners are possible. A p^+ sinker implant 36 similar as used in the prior art embodiment of figure 1 is shown on the left side of the source 34 of the left transistor. Such a p^+ sinker 36 can be created by ion implantation. Effectively, this p^+ sinker merges with the p well area 35 and, thus, reaches from the source runner

contact 33 to the backside metal layer 30. Contrary to the p^+ sinker 36, the p ring 20 surrounds or encloses the transistor structure. As shown in Figure 3, the p ring structure extends from the surface of the active area 1 downwards. Furthermore, the p ring 20 partially overlaps with the p^+ sinker and the source region 34 in areas 22 (see Fig. 2) where the source 34 and the p^+ sinker 36 are located. As indicated in figure 2, these areas 22 extend along the left and the right side of the drain regions 8, 9. Thus, the p ring 20 in Fig. 3 reaches from the surface into the active area in the areas 21 and 22 (as shown in Fig. 2) and encloses the combined transistor. Again, the p^+ sinker 36 can reach over the boundaries of the active area 1. However, the p ring 20 is completely located within the active area 1. As also indicated in Fig. 2, the p ring 20 can reach the right and left sides of the field oxide. (LOCOS edge). If no sinker structure is present, this can be done by designing the ring to extend from the left and right side into the active area. However, as shown in Fig. 2, if a p^+ sinker is used it will merge with the p ring 20 and thus, p ring 20 can extend to the edge of the field oxide.

Although particular embodiments of the invention have been shown and described, the invention is not limited to the preferred embodiments and it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention, which is defined only by the appended claims and their equivalents. For example, the embodiment shown describes a combined dual transistor arrangement. However, the principle of an insulating ring according to the present application can also be applied to structures with more than two transistors or to a single transistor structure. Furthermore, the substrate/epitaxial layer can be a p-type or an n-type substrate. Thus, source, drain region, the p ring, and other doped areas would be according to their function either of the n-type or the p-type.

Furthermore, the ring structure does not have to be in a rectangular form as shown in figure 2. Depending on the form of the transistor structure other suitable surrounding shapes can be used, such as a circle, oval, hexagonal, or any other polygon shape. Figure 4 A-F shows an exemplary variety of different ring shapes. For example, Fig.

4A depicts a circle shape, Fig. 4B a polygon shape, and Fig. 4D an oval shape. The main function is to insulate the electrical field. Therefore, depending on the structure of the transistor the ring might have some openings as long as they do not influence the substantially the shielding function. Fig. 4C, thus, shows another rectangular or square shape formed by four elements 40. These elements 40 can merge at their respective ends to form a continuous rectangular ring structure but also could have small gaps as long as the insulating function is kept. Fig. 4F shows another example, of a four element structure 42 with gaps at less critical areas of the ring. In Fig. 4E only two elements 41 are provided in the "horizontal" areas. These elements 41 merge with the p^+ sinker structures and, thus, form the insulating ring. Any other ring structure or combination of elements is possible to reach a similar result.